

ASSEMBLEUR

- ASSEMBLEUR - COMPLÉMENTS -

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Les registres

Les registres



Un exemple d'exécution

```
1129 eb 28 jmp 1153
... ..
1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
115a 48 c7 c3 03 00 00 00 mov $0x3,%rbx
1161 48 ff c3 inc %rbx
1164 e8 07 00 00 00 call 1170
1169 48 83 f8 63 cmp $0x63,%rax
116d 72 f5 jb 1161
116f c3 ret
1170 48 f7 e3 mul %rbx
1173 c3 ret
```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS				
...	0	0	0	0	0	0	0	0					

0	0	0	0	0	0	0	0	0	0	0	0	1	1	2	9	RIP
0	0	3	0	E	1	F	E	0	1	5	5	C	E	0	A	RAX
0	0	0	0	0	0	0	0	0	6	3	5	E	0	0	A	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5848															
...															
...															
000000000000e24a															

1

Un exemple d'exécution

```
• 1129 eb 28 jmp 1153
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1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS							
...	0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	0	0	0	0	0	1	1	2	9	RIP
0	0	3	0	E	1	F	E	0	1	5	5	C	E	0	A	RAX
0	0	0	0	0	0	0	0	0	6	3	5	E	0	0	A	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5848

...

...

000000000000e24a

←

..

..

2

Un exemple d'exécution

```
1129 eb 28 jmp 1153
... ..
• 1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS							
...	0	0	0	0	0	0	0	0								

0	0	0	0	0	0	0	0	0	0	0	0	1	1	5	3	RIP
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

0	0	3	0	E	1	F	E	0	1	5	5	C	E	0	A	RAX
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

0	0	0	0	0	0	0	0	0	6	3	5	E	0	0	A	RBX
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

00007ffdc10f5848																←
...																
...																
												000000000000e24a				

3

Un exemple d'exécution

1129 eb 28 jmp 1153
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1153 48 c7 c0 05 00 00 00 mov \$0x5,%rax
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Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS							
...	0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	0	0	0	0	0	1	1	5	a	RIP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RAX
0	0	0	0	0	0	0	0	0	6	3	5	E	0	0	A	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5848

...

...

000000000000e24a

..

..

4

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```
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116f c3 ret
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS															
...	0	0	0	0	0	0	0	0																
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	1	RIP							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RAX							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	3	RBX							
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP								

00007ffdc10f5848

...

...

000000000000e24a

..

..

5

Un exemple d'exécution

```
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... ..
1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
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```

Draft!



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```
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1173 c3 ret
```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS															
...	0	0	0	0	0	0	0	0																
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	7	0	RIP							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RAX							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	RBX							
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	0	RSP								

00007ffdc10f5840
00007ffdc10f5848
...
...

00000000000001169
0000000000000e24a
..
..



Un exemple d'exécution

```
1129 eb 28      jmp 1153
...          ...
1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
115a 48 c7 c3 03 00 00 00 mov $0x3,%rbx
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1164 e8 07 00 00 00 call 1170
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116d 72 f5      jb 1161
116f c3          ret
1170 48 f7 e3     mul %rbx
• 1173 c3          ret
```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF
...	0	0	0	0	0	0	1	0

RFLAGS

0	0	0	0	0	0	0	0	0	0	0	0	1	1	7	3
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

RIP

0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

RAX

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

RBX

0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

RSP

00007ffdc10f5840
00007ffdc10f5848

0000000000001169
000000000000e24a

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```
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... ..
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS				
...	0	0	0	0	0	0	1	0					

0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	9	RIP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4	RAX
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5840	00000000000001169
00007ffdc10f5848	0000000000000e24a ←
...	..
...	..

9

Un exemple d'exécution

```
1129 eb 28 jmp 1153
... ..
1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
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1161 48 ff c3 inc %rbx ←
1164 e8 07 00 00 00 call 1170
1169 48 83 f8 63 cmp $0x63,%rax
• 116d 72 f5 jb 1161 ←
116f c3 ret
1170 48 f7 e3 mul %rbx
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS															
...	0	0	0	1	0	0	0	1																

0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	d	RIP							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4	RAX							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	RBX							
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP							

00007ffdc10f5840																0000000000001169									
00007ffdc10f5848																000000000000e24a									
...																..									
...																..									

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Un exemple d'exécution

```
1129 eb 28 jmp 1153
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS				
...	0	0	0	1	0	0	0	1					

0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	1	RIP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4	RAX
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5840	00000000000001169
00007ffdc10f5848	0000000000000e24a
...	..
...	..

11

Un exemple d'exécution

1129 eb 28 jmp 1153
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1153 48 c7 c0 05 00 00 00 mov \$0x5,%rax
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Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS			
...	0	0	0	0	0	0	1	1				

0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	4	RIP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4	RAX
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5840	0000000000001169
00007ffdc10f5848	000000000000e24a
...	..
...	..

12

Un exemple d'exécution

```
1129 eb 28 jmp 1153
... ..
1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
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116f c3 ret
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS															
...	0	0	0	0	0	0	1	1																

0	0	0	0	0	0	0	0	0	0	0	0	1	1	7	0	RIP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4	RAX
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	0	RSP

00007ffdc10f5840
00007ffdc10f5848
...
...

0000000000001169
000000000000e24a
..
..

←

13

Un exemple d'exécution

```
1129 eb 28 jmp 1153
... ..
1153 48 c7 c0 05 00 00 00 mov $0x5,%rax
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1169 48 83 f8 63 cmp $0x63,%rax
116d 72 f5 jb 1161
116f c3 ret
1170 48 f7 e3 mul %rbx
• 1173 c3 ret
```

Draft!

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...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS											
...	0	0	0	0	0	0	0	0												
0	0	0	0	0	0	0	0	0	0	0	0	1	1	7	3	RIP				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	4	RAX				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX				
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	0	RSP				

00007ffdc10f5840
00007ffdc10f5848
...
...

0000000000001169
000000000000e24a
..
..

←

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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS							
...	0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	0	0	0	0	1	1	6	9	RIP	
0	0	0	0	0	0	0	0	0	0	0	0	0	6	4	RAX	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX	
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP

00007ffdc10f5840
00007ffdc10f5848
...
...

0000000000001169
000000000000e24a
..
..

15

Un exemple d'exécution

```
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS							
...	0	0	0	0	0	0	0	0	0							

0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	d	RIP
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	4	RAX
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	-----

00007ffdc10f5840
00007ffdc10f5848
...
...

0000000000001169
000000000000e24a
..
..

16

Un exemple d'exécution

```
1129 eb 28 jmp 1153
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Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS															
...	0	0	0	0	0	0	0	0																
0	0	0	0	0	0	0	0	0	0	0	0	1	1	6	f	RIP								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	4	RAX								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX								
0	0	0	0	7	f	f	d	c	1	0	f	5	8	4	8	RSP								

00007ffdc10f5840
00007ffdc10f5848
...
...

0000000000001169
000000000000e24a
..
..

17

Un exemple d'exécution

```
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```

Draft!

...	OF	DF	TF	SF	ZF	AF	PF	CF	RFLAGS															
...	0	0	0	0	0	0	0	1																

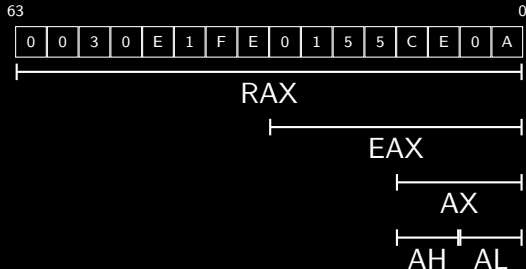
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	RIP							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	4	RAX							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	5	RBX							
0	0	0	0	7	f	f	d	c	1	0	f	5	8	5	0	RSP								

00007ffdc10f5840	00000000000001169
00007ffdc10f5848	0000000000000e24a
...	..
...	..

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General purpose registers :

Registers	Lower dword	Lower word	Lower byte	Name	common usage
rax	eax	ax	al	Accumulator	It is used for I/O port access, arithmetic, interrupt calls



Draft!

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Registers	Lower dword	Lower word	Lower byte	Name	common usage
rax	eax	ax	al	Accumulator	It is used for I/O port access, arithmetic, interrupt calls
rbx	ebx	bx	bl	Base	Base pointer for memory access
rcx	ecx	cx	cl	Counter	loop counter
rdx	edx	dx	dl	Data	I/O port access, arithmetic, some interrupt
r8	r8d	r8w	r8b		
r9	r9d	r9w	r9b		
r10	r10d	r10w	r10b		
r11	r11d	r11w	r11b		
r12	r12d	r12w	r12b		
r13	r13d	r13w	r13b		
r14	r14d	r14w	r14b		
r15	r15d	r15w	r15b		

Draft!

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rcx	ecx	cx	cl	Counter	loop counter
rdx	edx	dx	dl	Data	I/O port access, arithmetic, some interrupt
r8	r8d	r8w	r8b		
r9	r9d	r9w	r9b		
r10	r10d	r10w	r10b		
r11	r11d	r11w	r11b		
r12	r12d	r12w	r12b		
r13	r13d	r13w	r13b		
r14	r14d	r14w	r14b		
r15	r15d	r15w	r15b		

Segment registers (and selectors) : cs, ds, es, fs, gs, ss.

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registers :

Registers	Lower dword	Lower word	Lower byte	Name	common usage
rsp	esp	sp	spl	Stack pointer	Holds the top address of the stack
rsi	esi	si	sil	Source index	memory array copying and setting
rdi	edi	di	dil	Destination index	memory array copying and setting
rbp	ebp	bp	bpl	Stack Base pointer	Holds the base address of the stack
rip	eip	ip		Index Pointer?? instruction pointer?	Holds the offset of the next instruction

Flags registers :

Draft !

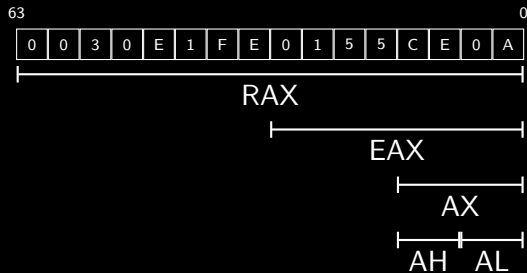
...	OF	DF	TF	SF	ZF	AF	PF	CF
...	0	0	0	0	0	0	1	1

RFLAGS

CF	Carry flag	TF	Trap flag
PF	Parity flag	IF	Interrupt enable flag
AF	Auxiliary Carry flag	DF	Direction flag
ZF	Zero flag	OF	Overflow flag
SF	Sign flag	...	...

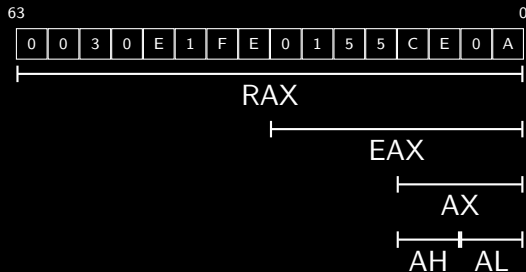
- Updated by many instructions (cmp, or, test...) but not all (mov).
- Influences some instructions (je, jz, j..., cmov, setc, ...) and even prefix (repz, rep...).
- you can not set it directly (no mov) but you can push/pop it to/from the stack.

Draft!



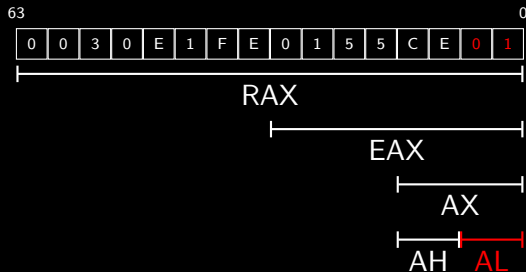
Draft !

```
...  
ba06b133 b0 01 movb $1, %al  
ba06b135 b4 02 movb $2, %ah  
ba06b137 66 b8 04 00 movw $4, %ax  
ba06b13b b8 08 00 00 00 movl $8, %eax  
ba06b140 48 c7 c0 10 00 00 00 movq $16, %rax  
ba06b147 48 b8 50 eb 12 a1 25 00 00 00 movabsq ..., %rax
```



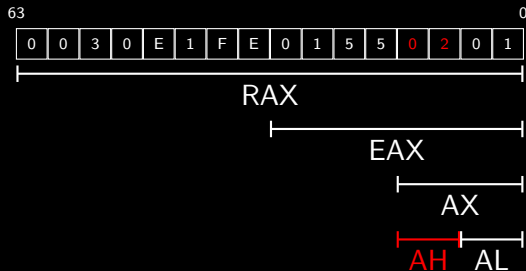
Draft !

- | ... | ... | ... |
|----------|----------------|-------------------|
| ba06b133 | b0 01 | movb \$1, %al |
| ba06b135 | b4 02 | movb \$2, %ah |
| ba06b137 | 66 b8 04 00 | movw \$4, %ax |
| ba06b13b | b8 08 00 00 00 | movl \$8, %eax |
| ba06b140 | 48 c7 c0 10 00 | movq \$16, %rax |
| | 00 00 | |
| ba06b147 | 48 b8 50 eb 12 | movabsq ..., %rax |
| | a1 25 00 00 00 | |



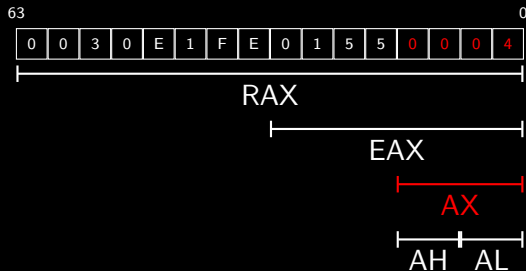
Draft !

...	...	...
ba06b133	b0 01	movb \$1, %al
• ba06b135	b4 02	movb \$2, %ah
ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq ..., %rax
	a1 25 00 00 00	



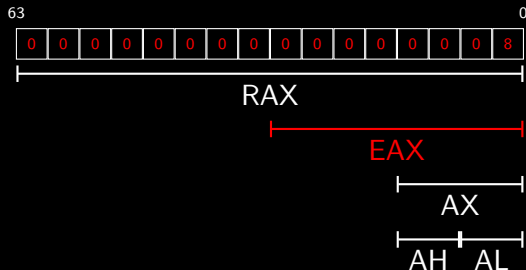
Draft !

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
• ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq ..., %rax
	a1 25 00 00 00	



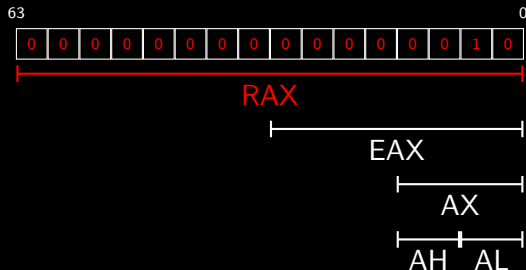
Draft !

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
ba06b137	66 b8 04 00	movw \$4, %ax
• ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq ..., %rax
	a1 25 00 00 00	



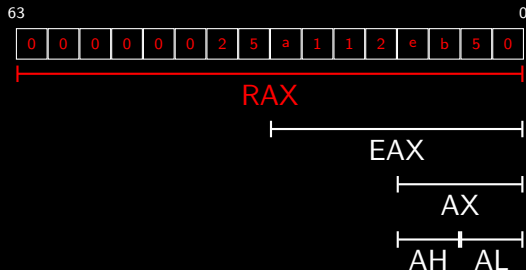
Draft !

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
• ba06b140	48 c7 c0 10 00 00 00	movq \$16, %rax
ba06b147	48 b8 50 eb 12 a1 25 00 00 00	movabsq ..., %rax



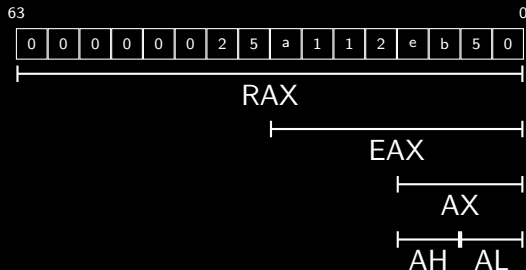
Draft !

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
• ba06b147	48 b8 50 eb 12	movabsq ..., %rax
	a1 25 00 00 00	



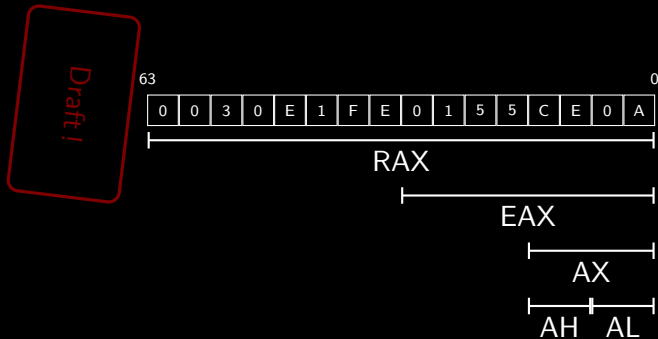
Draft !

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq .., %rax
	a1 25 00 00 00	



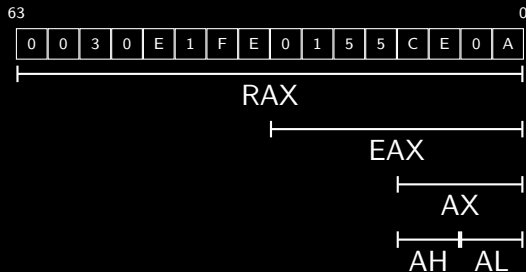
SIMD registers : *Draft !*

Extension	Registers	size	Numbers	Common usage
MMX	mm0–mm7	64 bits	8	Entiers (obsolete)
SSE	xmm0–xmm15	128 bits	16	SIMD générique
AVX	ymm0–ymm15	256 bits	16	SIMD large
AVX-512	zmm0–zmm31	512 bits	32	SIMD très large
AVX-512	k0–k7	64 bits	8	Masques de prédication
AMX	tmm0–tmm7	512 bits (Jusqu'à 1024 B / tile)	8	Calcul matriciel (IA, HPC)
AMX	tilecfg	Structure de config	1	Décrit les tailles de tuiles



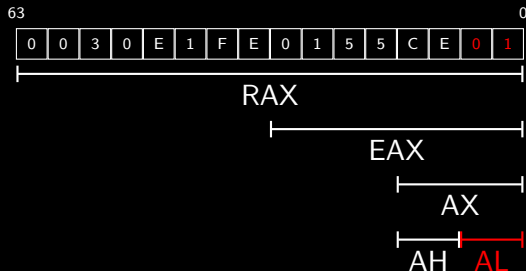
Draft!

```
...  
ba06b133 b0 01 movb $1, %al  
ba06b135 b4 02 movb $2, %ah  
ba06b137 66 b8 04 00 movw $4, %ax  
ba06b13b b8 08 00 00 00 movl $8, %eax  
ba06b140 48 c7 c0 10 00 00 00 movq $16, %rax  
ba06b147 48 b8 50 eb 12 movabsq ..., %rax  
a1 25 00 00 00
```



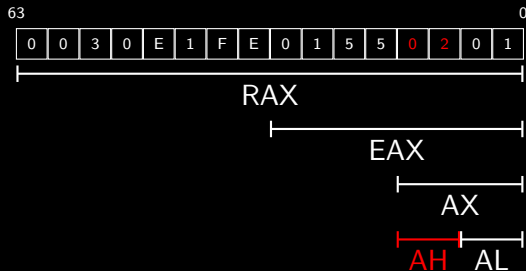
Draft!

- ...
ba06b133 b0 01 movb \$1, %al
ba06b135 b4 02 movb \$2, %ah
ba06b137 66 b8 04 00 movw \$4, %ax
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ba06b140 48 c7 c0 10 00 00 00 movq \$16, %rax
ba06b147 48 b8 50 eb 12 movabsq .., %rax
a1 25 00 00 00



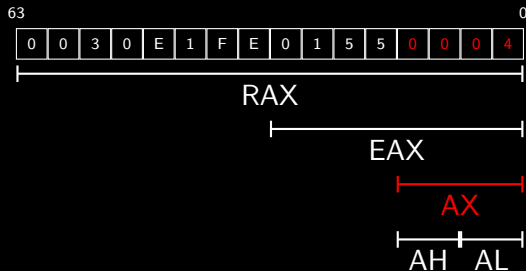
Draft!

...	...	...
ba06b133	b0 01	movb \$1, %al
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ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq ..., %rax
	a1 25 00 00 00	



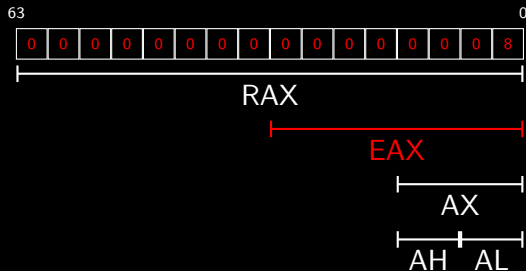
Draft!

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
• ba06b137	66 b8 04 00	movw \$4, %ax
ba06b13b	b8 08 00 00 00	movl \$8, %eax
ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq .., %rax
	a1 25 00 00 00	



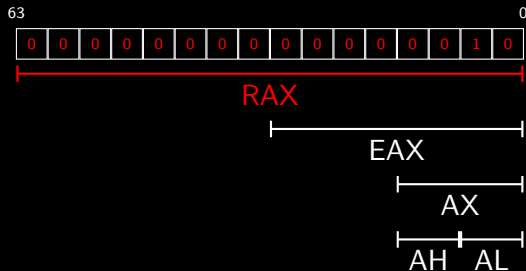
Draft!

...	...	...
ba06b133	b0 01	movb \$1, %al
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ba06b140	48 c7 c0 10 00	movq \$16, %rax
	00 00	
ba06b147	48 b8 50 eb 12	movabsq .., %rax
	a1 25 00 00 00	



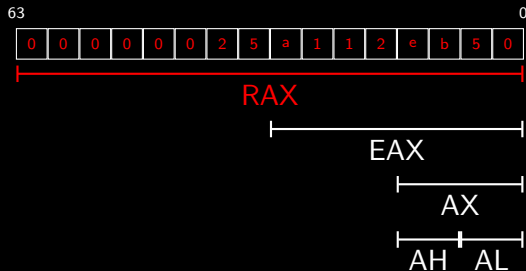
Draft!

...	...	...
ba06b133	b0 01	movb \$1, %al
ba06b135	b4 02	movb \$2, %ah
ba06b137	66 b8 04 00	movw \$4, %ax
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Draft!

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	00 00	
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	a1 25 00 00 00	



Draft!

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	00 00	
ba06b147	48 b8 50 eb 12	movabsq .., %rax
	a1 25 00 00 00	

